REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

In the Office Action dated May 12, 2005, the Examiner requested that the applicants affirm the election of Group I, i.e., Claims 1-18 that was made, without traverse, by applicants' previous representative Eric W. Petraske on April 26, 2005. Responsive to this request, the undersigned hereby affirms the previous election of Claims 1-18. Accordingly, Claims 1-18 are pending and Claims 19-20 are withdrawn.

Before addressing the specific grounds of rejection raised in the Office Action, applicants have amended the specification to include a description of reference numeral 13 which appears in FIGS. 6 –9 of the original filed application. Specifically, applicants have amended the paragraph appearing at paragraph 0034 of the published application to include a statement that "reference numeral 13 denotes an oxidized portion of the back gate electrode." This is supported in the paragraph appearing at paragraph 0034 of the published application since an oxidation process is described therein. Attention is also directed to original Claim 19 which also positively recites an oxide layer being present within the back gate electrode.

In addition, applicants have also amended Claims 1 and 2 by changing the term "Device layer" to "device layer".

Applicants respectfully submit that the amendments to the specification and claims do not introduce new matter into the originally filed application. As such, entry of the foregoing amendments to the specification and claims is respectfully requested.

Claims 1-5 and 9-11 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of U.S. Patent No. 6,465,823 to Yagishita et al. ("Yagishita et al.") and

U.S. Patent No. 5,712,173 to Liu et al. ("Liu et al."). Claim 16 stands rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Yagishita et al., Liu et al. and U.S. Patent No. 5,891,798 to Doyle et al. ("Doyle et al."). Claim 6-8 and 12-13 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Yagishita et al., Liu et al., and U.S. Patent No. 6,117,711 to Wu ("Wu"). Claims 15-17 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Yagishita et al., Liu et al., Wu and Doyle et al. Claim 18 stands rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Yagishita et al., Liu et al., and Wolf, Silicon Processing for VLSI Era, Vol. 4, Lattice Press (2002).

Applicants respectfully submit that the claims of the present application are not rendered obvious by the combination of applied references cited in the Office Action dated May 12, 2005. Specifically, none of the applied references teach or suggest a method of fabricating a double-gate transistor in which a portion of the back gate electrode has been oxidized such that an oxide 13 is formed below the transistor body 4 and on either side of a central portion of the back gate electrode 2, as presently claimed in method Claims 1-18.

The primary reference, i.e., Yagishita et al., spurring each of the obvious rejections is defective in that the reference does not teach or suggest the fabrication of a double-gate transistor, let alone a method in which a portion of the back gate electrode has been oxidized as presently claimed. Yagishita et al. discloses methods of forming a metal insulator semiconductor field effect transistor (MISFET) which includes a single gate electrode 1009. The top of the single gate electrode 1009 is in contact with a lower portion 1030a of an SOI layer 1003 by contact 1012. Applicants observe that Yagishita et al. does not teach or suggest the presence of a second gate electrode which, together with a second gate dielectric, are required for fabricating a

double-gate transistor. Applicants observe that the Examiner appears to suggest that the SOI substrate layer 1001 is the back gate electrode. This statement is unfounded since Yagishita et al. does not teach or suggest that the substrate layer 1001 is a gate electrode and nowhere in the applied reference does it teach or suggest a step of oxidizing a back gate electrode, or even the substrate 1001.

Applicants submit that in order for the substrate 1001 of Yagishita et al. to function as a back gate electrode it must be doped to include a dopant concentration that is sufficient for that layer to function as a gate electrode. Yagishita et al. does not teach or suggest such doping and as such the applied reference does not teach or suggest the formation of a double-gate transistor, as presently claimed.

Applicants submit that none of the applied secondary references, namely, Liu et al., Wu, Doyle and Wolf, alleviate the above defects in Yagishita et al. since those applied references also do not teach or suggest a method of fabricating a double-gated transistors including the claimed processing steps recited in Claims 1-18. Applicants observe that Liu et al. and Wu both discloses methods of fabricating a single gated transistor. Applicants submit that methods of fabricating a single gated device are different than methods used in forming double-gated devices and, as such, one skilled in the art would not necessarily consider to combine such technologies.

Doyle et al. does mention that substrate 300 can be a conductor, but that prior art reference does not teach or suggest oxidizing a portion of the back gate electrode as presently claimed.

Wolf, which is applied to Claim 18, also does not teach or such applicants' claimed processing steps which provide a double-gate transistor.

In view of the above remarks, the obviousness rejections have been obviated. Reconsideration and withdrawal of each of the obviousness rejections is thus respectfully requested.

The various §103 rejections also fail because there is no motivation in the applied references which suggest modifying the disclosed methods to include the various elements, in particular formation of a double-gated transistor, recited in the claims of the present invention. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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